Notice of Allowability	Application No. 10/685,042	Applicant(s) CAMERLO ET AL.	
	Examiner Ishwar (I. B.) Patel	Art Unit 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *February 3, 2006 and interview summary*.

2. ☒ The allowed claim(s) is/are *1,3-5 ,7-11 and 13-19*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *030206* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Jeffrey J. Duquette (Reg. 45,487) on February 23, 2006.

The application has been amended as follows: Amend the claims as below:

1. (Currently Amended) A pad layout for mounting with a circuit board component, the pad layout comprising:

a set of pads arranged on a surface of a circuit board in a two-dimensional array having at least two pads in a first direction and at least two pads in a second direction that is substantially perpendicular to the first direction, each pad of the set of pads having (i) a central portion and (ii) multiple lobe portions integrated with the central portion and extending from the central portion of that pad;

a solder mask on the surface of the circuit board, the solder mask extending around a periphery of each pad of the set of pads, the solder mask defining a set of apertures, each aperture having (i) a central aperture portion and (ii) multiple lobe aperture portions integrated with the central aperture portion to mirror a profile of a corresponding pad, the solder mask defining clearance regions around each pad of the set of pads;

wherein, for each pad of the set of pads, that pad has exactly four lobe portions that extend from the central portion of that pad;

wherein the circuit board component includes an integrated circuit package and multiple pre-soldered contacts extending from the integrated circuit package; and wherein the set of pads provide multiple metallic surfaces configured to simultaneously solder to the multiple pre-soldered contacts of the circuit board component during a circuit board assembly process involving printing solder paste onto the multiple metallic surfaces, picking and placing the circuit board component onto the solder paste and applying heat; and

wherein, for each pad of the set of pads, (i) each lobe portion defines a distally disposed edge which is convex relative to a center of that pad, (ii) each central portion define central portion edges which are concave relative to the center of that pad, (iii) the distally disposed edges and the central portion edges blend smoothly in a manner that is free of sharp angled intersections, and (iv) each concave edge has a radius which is at least twice as large in value as a radius of every convex edge.

6. (Cancel).

7. (Currently Amended) The pad layout of claim [[6]] 1 wherein the solder mask ~~further~~ defines clearance regions that are substantially 2 mils wide around each pad of the set of pads.

11. (Currently Amended) A circuit board, comprising:

a set of circuit board layers combined to form a rigid planar structure having an outer surface; and

a pad layout configured to mount with a circuit board component, the pad layout including a set of pads arranged on the surface of a circuit board in a two-dimensional array having at least two pads in a first direction and at least two pads in a second direction that is substantially perpendicular to the first direction, each pad of the set of pads having (i) a central portion and (ii) multiple lobe portions integrated with the central portion and extending from the central portion of that pad;

a solder mask on the surface of the circuit board, the solder mask extending around a periphery of each pad of the set of pads, the solder mask defining a set of apertures, each aperture having (i) a central aperture portion and (ii) multiple lobe aperture portions integrated with the central aperture portion to mirror a profile of a corresponding pad, the solder mask defining clearance regions around each pad of the set of pads;

wherein, for each pad of the set of pads, that pad has exactly four lobe portions that extend from the central portion of that pad, two of the four lobe portions of that pad extending along a first axis, and another two of the four lobe portions of that pad extending along a second axis that is substantially perpendicular to the first axis;

wherein the circuit board component includes an integrated circuit package and multiple pre-soldered contacts extending from the integrated circuit package; and wherein the set of pads provide multiple metallic surfaces configured to simultaneously solder to the multiple pre-soldered contacts of the circuit board component during a circuit board assembly process involving printing solder paste onto the multiple metallic surfaces, picking and placing the circuit board component onto the solder paste and applying heat; and

wherein, for each pad of the set of pads, (i) each lobe portion defines a distally disposed edge which is convex relative to a center of that pad, (ii) each central portion define central portion edges which are concave relative to the center of that pad, (iii) the distally disposed edges and the central portion edges blend smoothly in a manner that is free of sharp angled intersections, and (iv) each concave edge has a radius which is at least twice as large in value as a radius of every convex edge.

14. (Currently Amended) The circuit board of claim 11, ~~further comprising:~~

~~solder mask on the surface of the circuit board, the solder mask extending around a periphery of each pad of the set of pads, the solder mask defining a set of apertures, each aperture having (i) a central aperture portion and (ii) multiple lobe aperture portions integrated with the central aperture portion to mirror a profile of a corresponding pad,~~ the solder mask ~~further~~ defining clearance regions that are substantially 2 mils wide around each pad of the set of pads.

16. (Currently Amended) A circuit board assembly, comprising:

a set of circuit board layers combined to form a rigid planar structure having an outer surface;

a pad layout including a set of pads arranged on the surface of a circuit board in a two-dimensional array having at least two pads in a first direction and at least two pads in a second direction that is substantially perpendicular to the first direction, each pad of the set of pads having (i) a central portion and (ii) multiple lobe portions integrated with the central portion and extending from the central portion of that pad;

a solder mask on the surface of the circuit board, the solder mask extending around a periphery of each pad of the set of pads, the solder mask defining a set of apertures, each aperture having (i) a central aperture portion and (ii) multiple lobe aperture portions integrated with the central aperture portion to mirror a profile of a corresponding pad, the solder mask defining clearance regions around each pad of the set of pads;

a circuit board component mounted to the pad layout via a set of solder joints;

wherein, for each pad of the set of pads, that pad has exactly four lobe portions that extend from the central portion of that pad;

wherein the circuit board component includes an integrated circuit package and multiple pre-soldered contacts extending from the integrated circuit package, and wherein the set of pads provide multiple metallic surfaces configured to simultaneously solder to the multiple pre-soldered contacts of the circuit board component during a circuit board assembly process involving printing solder paste onto the multiple metallic surfaces, picking and placing the circuit board component onto the solder paste and applying heat; and

wherein, for each pad of the set of pads, (i) each lobe portion defines a distally disposed edge which is convex relative to a center of that pad, (ii) each central portion define central portion edges which are concave relative to the center of that pad, (iii) the distally disposed edges and the central portion edges blend smoothly in a manner that is free of sharp angled intersections, and (iv) each concave edge has a radius which is at least twice as large in value as a radius of every convex edge.

19. (Currently Amended) A circuit board assembly, comprising:

a set of circuit board layers combined to form a rigid planar structure having an outer surface;

a pad layout including a set of pads arranged on the surface of a circuit board in a two-dimensional array having at least two pads in a first direction and at least two pads in a second direction that is substantially perpendicular to the first direction, each pad of the set of pads having (i) a central portion and (ii) multiple lobe portions integrated with the central portion and extending from the central portion of that pad;

a solder mask on the surface of the circuit board, the solder mask extending around a periphery of each pad of the set of pads, the solder mask defining a set of apertures, each aperture having (i) a central aperture portion and (ii) multiple lobe aperture portions integrated with the central aperture portion to mirror a profile of a corresponding pad, the solder mask defining clearance regions around each pad of the set of pads;

a circuit board component;

means for mounting the circuit board component to the set of pads of the pad layout;

wherein, for each pad of the set of pads, that pad has exactly four lobe portions that extend from the central portion of that pad;

wherein the circuit board component includes an integrated circuit package and multiple pre-soldered contacts extending from the integrated circuit package; and wherein the set of pads provide multiple metallic surfaces configured to simultaneously solder to the multiple pre-soldered contacts of the circuit board component during a circuit board assembly process involving

printing solder paste onto the multiple metallic surfaces, picking and placing the circuit board component onto the solder paste and applying heat; and

wherein, for each pad of the set of pads, (i) each lobe portion defines a distally disposed edge which is convex relative to a center of that pad, (ii) each central portion define central portion edges which are concave relative to the center of that pad, (iii) the distally disposed edges and the central portion edges blend smoothly in a manner that is free of sharp angled intersections, and (iv) each concave edge has a radius which is at least twice as large in value as a radius of every convex edge.

2. The following is an examiner's statement of reasons for allowance: Regarding claims 1, 3-5, 7-11 and 13-19, the patentability resides in the limitations "(wherein), for each pad of the set of pads, that pad has exactly four lobe portions that extend from the central portion of that pad" and "(w)herein for each pad of the set of pads, (i) each lobe

portion defines a distally disposed edge which is convex relative to a center of that pad, (ii) each central portion define central portion edges which are concave relative to the center of that pad, (iii) the distally disposed edges and the central portion edges blend smoothly in a manner that is free of sharp angled intersections, and (iv) each concave edge has a radius which is at least twice as large in value as a radius of every convex edge," in combination with other claimed limitations of the base claims 1, 11, 16 and 19.

The prior art, taken alone, or in combination does not fairly teach or suggest all the limitations of the structure in the manner as claimed by the base claims 1, 11, 16 and 19.

The closest prior of Natarajan et al., (US Patent No. 5,519,580) discloses a pad structure in figure 3, but does not disclose the concave edge as claimed or the relation between the radius of the concave edge and the convex edge as claimed, Darveaux et al. (US Patent No. 6,201, 305) discloses pad structure in figure 3A-4A, but does not disclose the radius of the concave edge at least twice as large as a radius of every convex edge, Lee, (US Patent No. 5,872,399) disclose pad structure in figure 4, but does not recites the radius of the concave edge at least twice as large as a radius of every convex edge. Further, none of the above art recites the mask openings arrangement around the pads as claimed by the applicant.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ishwar (I. B.) Patel
Patent Examiner
Art Unit: 2841
March 2, 2006